EVALUATION OF PCM TOLL SWITCHING NETWORKS WITH PARTIAL ACCESS PULSE SHIFTERS
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ABSTRACT
PCM switching may be considered as a feasible solution to a large-scale toll telephone office in such circumstances that the toll traffic demand is ever increasing and that PCM transmission systems are being installed in larger numbers. The present paper describes an economical approach to the realization of large-scale PCM toll switching networks by employing partial access pulse shifters which perform channel interchange within a fraction of a frame and thereby reduce the amount of required memory capacity. Optimization of three categories of networks, namely the serial PCM switching, the bit-interleaved PCM switching and the parallel PCM switching, is made and the optimized networks of three categories are compared with reference to such network parameters as the time-division multiplexity, the number of trunks, the channel accessibility and the gate-memory cost ratio.

1. INTRODUCTION
Ever since the concept of integrating transmission and switching by pulse code modulation (PCM) techniques emerged with the ESSEX system, various studies have been made on the application of the concept to local switching, tandem switching and toll switching. In the mean time, PCM transmission systems are rapidly in use supported by the remarkable progress of digital device technology. High rate of increase of toll traffic demand on the other hand, calls for a large-scale toll telephone offices. In these prevailing circumstances, it may seem reasonable to introduce PCM toll offices which can handle up to several ten thousand Erlangs in the nodes of higher hierarchy where interfacing to electromechanical subsets is not an essential factor. The PCM links connecting these nodes may be the secondary groups with the time-division multiplexity of 96 or more rather than the primary groups with 24 or 32 channels.

The channel interchange capability is indispensable in PCM toll switching network in which the channels are preassigned in originating offices and average trunk loading is quite high. The channel interchange device or the "pulse shifter" was originally to store the channel pulses in an entire frame and in reading out the contents in specific order, provide access to any channel in a frame. As for the channel accessibility or the number of interchangeable channels, however, 10 to 20 is found to be generally sufficient even if the average trunk loading is 0.7 or more. This indicates that the prototype pulse shifters are unnecessary and uneconomical if applied to the secondary groups having 96 or more channels in a frame. From this point of view, the discussion in the present paper is concentrated on the use of various types of partial access pulse shifters which provide access to channels within a fraction of a frame which is called in this paper as a subframe.

The partial access pulse shifters may assume a variety of configurations depending upon the transmission format of the secondary groups as well as the switching format. A secondary group of n channels may be composed by interleaving channel-wise m primary groups each with n/m channels. Such secondary group assumes the familiar serial PCM format as shown in Fig. 1(b). Where b is the number of coded speech bits per channel. Or m primary groups each with n/m channels may be interleaved bit-wise to form a secondary group of n channels as shown in Fig. 1(c). The serial PCM may be switched serially, or may be switched in parallel by...
providing serial-to-parallel and parallel-to-serial converters at the input and the output of the switching network. The bit interleaved PCM trunks may be switched in the same format. There might be some other combinations of transmission and switching format which are beyond the scope of the present discussion, although not much economy may be gained or some difficulty in realization may be encountered especially in the case of parallel transmission.

The present paper is intended to find out the optimum design of the above-mentioned three categories of switching networks all with partial access pulse shifters, and to compare the economy between the optimized networks with respect to such network parameters as the time-division multiplexity, the number of trunks, the channel accessibility and the gate-memory cost ratio. The optimization is performed by minimizing relative cost of the switching network while maintaining the overall blocking probability to less than 1%.

2. PARTIAL ACCESS PULSE SHIFTERS AND THEIR CONTROL

Connection from the calling to the called subscriber as well as that from the called to the calling subscriber should be set up in telephone switching. In a PCM switching system which is inherently four wire, the forward and the backward speech paths are generally provided by means of two identical networks in which the same channel of the corresponding part of the networks is used in transmitting speech signal in forward and backward directions. If a pulse shifter for forward connection shifts the i-th channel to the j-th channel, the corresponding pulse shifter for the backward connection therefore shifts the j-th channel to the i-th. As has been described, reasonable overall blocking probability can be maintained when the channels can be interchanged are limited within a certain fraction of a frame. This suggests the possibility of reducing the required capacity of speech memories which, otherwise amounts to (n - 1) channels. The conventional method of channel interchange, however, does not accomplish this as is illustrated in Fig. 2(a). It may be apparent from the figure that, even if the i-th channel is to be shifted to the j-th channel within a subframe, the corresponding shift from the j-th channel to the i-th channel requires a delay of (n - j + i) channel intervals which may amount to (n - 1) channel intervals in such extreme case as j = i + 1.

The reduction of memory capacity is realized by modifying the relationship between the input and the output timing. Fig. 2(b) shows the operational timing of a pair of partial access pulse shifters for serial PCM switching as a typical example. To interchange the i-th channel to the j-th, a pulse shifter delays the i-th channel to the j-th channel in the succeeding subframe and the other pulse shifter in pair delays the j-th channel to the i-th channel in the succeeding subframe. Thus a subframe at the output of a pulse shifter occurs one subframe period later than the corresponding subframe at its input. A pulse shifter performing this operation therefore requires a delay of (2m - 1) channel intervals which is smaller than (n - 1) channel intervals if m < \(\frac{n}{2}\).

2.1 PARTIAL ACCESS PULSE SHIFTERS FOR SERIAL PCM SWITCHING

The operation of the pulse shifter may be understood with reference to Fig. 3(a). The pulse shifter for forward connection, which is shown in upper half of the diagram, stores the first, the second, \(\ldots\), and the \((m - 1)\) th channels in a subframe into the input shift register, and during the \(m\) th channel, transfers the stored and the arriving channels into \(m\) output shift registers. During the succeeding subframe, the pulse shifter control opens the gates associated with the output shift registers in specific order so that the stored channels are read out in specific output channels. The pulse shifter for the backward connection shown in the lower half of the diagram stores \(m\) channels in a subframe in a specific order as directed by the pulse shifter control into \(m\) input shift registers. During the succeeding subframe, the stored channels are read out and sent, through the output shift register providing delay of up...
to \((m-1)\) channels, to the output bus. The timing diagram shown in the figure clearly indicates that the synchronization between the output of the pulse shifter for forward connection and the input of the pulse shifter for backward connection permits the use of single pulse shifter control to commonly control the gates associated with the output shift registers of the former and the gates associated with the input shift registers of the latter. For instance, the \(i\)th input channel of the pulse shifter for forward connection is shifted to its \(j\)th output channel, and the \(j\)th input channel of the pulse shifter for backward connection is shifted to its \(i\)th output channel by commonly applying a control signal which opens the \(i\)th gate in the \(j\)th channel.

The number of components needed for the above described pair of pulse shifters is as follows. The memories are \((2m-1)b\) bits for storing speech signals, \([\log_2 (m+1)]\) bits for selecting gates and \(n[\log_2 (m+1)]\) bits for storing control signal for each channel constituting a frame. The gates are \(4m\) for speech paths, \(m\) for decoding and \([\log_2 (m+1)]\) for transferring control information from the control signal store to the gate selector. The notation \(\lfloor x \rfloor\) indicates the fraction of its content is raised.

Fig. 3(b) shows the configuration when the output of the pulse shifter for forward connection is not synchronized with the input of the pulse shifter for backward connection. In this case, pulse shifter controls should be individually provided to each pulse shifter and the output of the control signal store is applied first to the pulse shifter in advanced timing and then transferred to the other pulse shifter to provide necessary delay. The required numbers of components are the same for the speech memory, the control signal store, the speech path gates and the transfer gates, but are doubled for the gate selector and the decoder. The numbers of components required for the configurations of Figs. 3(a) and 3(b) are summarized in the first columns of Tables 1(a) and 1(b) respectively.

2.2 PARTIAL ACCESS PULSE SHIFTER FOR BIT INTERLEAVED PCM SWITCHING

As shown in Fig. 4(a), \(m\) primary groups are bit interleaved into a secondary group of \(n\) channels so that one bit intervals of a primary group is subdivided into \(m\) minor bit intervals and that \(b\) bits constituting one channel appears in \(m\) minor bit intervals successively \(b\) times. The channel interchange is performed within \(m\) channels so that the same interchange pattern repeats \(b\) times. The subframe in this case is therefore \(m\) minor bits belonging to one bit interval of a primary group.

The pulse shifter shown in the upper half of Fig. 4(b) is for the forward connection. It stores \(m\) minor bits in the input shift register and, at the end of the subframe, transfers the contents to the output shift register. During the succeeding subframe, the contents of the output shift register are read out through the associated gates in the specific order as directed by the pulse shifter control. The pulse shifter for the backward connection which is shown in the lower half of the diagram, stores the \(m\) minor bits into the input shift register through the associated gates in the specific order as directed by the pulse shifter control, and at the end of the subframe transfers the contents into the output register the contents of which are then successively read out during the succeeding subframe.

The required numbers of memory bits for the control signal store and of speech gates and decoder gates are the same to that for the serial PCM switching, although the speech memory bits are only \(4m\). The required numbers of memory bits for the gate selector and of transfer gates on the other hand, are \(m\) times as are compared to those for the serial PCM switching. As is shown in the figure, the contents of the gate selectors are recirculated for \(b\) times to perform the same operation to complete channel interchange. The required numbers of components are summarized in the second columns of Tables 1(a) and 1(b) for the synchronized case and the unsynchronized case respectively.

2.3 PARTIAL ACCESS PULSE SHIFTER FOR PARALLEL PCM SWITCHING

Fig. 5 shows the pulse shifters in this case when the parallel output of the pulse shifter for the forward connection is synchronized with the parallel input of the pulse shifter for the backward connection. As shown in the upper half of the figure, a serial to parallel conversion pulse shifter for the forward connection accommodates \(r\) serial PCM trunks, stores \(m\) channels each from the serial trunks into the shift registers and reads out the contents in the succeeding subframe in parallel into the parallel bus as specified by the pulse shifter control. Two shift registers are provided to each serial trunk, one storing while the other is being read out. The pulse shifter performs interchange among \(m\) parallel channels.
The parallel to serial conversion pulse shifter for the backward connection is shown in the lower half of the figure. As directed by the pulse shifter control, the parallel channels are stored in specific memory positions so that when serially read out, each speech signal occupies the specific channel in specific serial trunk.

The required numbers of components per input-output trunk pair are shown in the third columns of Tables 1(a) and 1(b) for the synchronized and unsynchronized cases respectively.

### 3. JUNCTOR GATES AND THEIR CONTROL

A pair of junctors, one in the forward path and the other in the backward path, transmit speech in opposite directions to provide a telephone conversation. If a pair of junctors are synchronized, or in other words, the forward and the backward information in the same channel coincides, the junctor gates connected to the pair of junctors can be controlled by a common junctor gate control. If not, the junctor gates for the forward path and that for the backward path must be controlled individually by two junctor gate controls.

In case that \( k \) and \( l \) are connected and \( k \) is larger than \( l \), the junctor gate controls should preferably be provided to each of \( l \) junctors and used to specify, for each channel, one out of \( k \) junctors to be connected. This requires \( \log_2(k+1) \) bits of information which is apparently smaller than \( k \log_2(l+1) \) bits that are required otherwise.

#### 3-1 JUNCTOR GATES FOR SERIAL PCM SWITCHING

Fig. 6(a) shows a pair of the junctor gates and their control when the forward and the backward paths are synchronized. As shown in the figure 2 \( k \) junctor gates are needed to provide the forward and backward speech paths to and from a pair of \( k \) junctors. The junctor gate control requires \( \log_2(k+1) \) bits of memory for gate control to specify for each channel, one out of \( k \) junctors to be connected. In addition \( n \log_2(k+1) \) bits of memory is required to store the information for each channel. The junctor gate control also requires \( \log_2(k+1) \) gates for decoding the output of the gate control. These are summarized in the first column of Table 2(a).

Fig. 6(b) shows the case that the forward and the backward paths are not synchronized. Since the junctors to be connected must be specified individually in forward and backward paths.

### 3-2 JUNCTOR GATES FOR BIT INTERLEAVED PCM SWITCHING

The configuration of the junctor gates and their control for the bit interleaved PCM switching is basically the same to that for the serial PCM switching except for the fact that, in contrast to the latter in which the junctor gates are controlled for the duration of \( b \) bits constituting a channel, the former requires the gate control to be performed repeatedly \( b \) times with \( m \) minor bits interval. As the result, the control information for \( m \) channels is to be read out to a recirculating memory and recirculated there \( b \) times. Fig. 7 shows the configuration in case that the forward and the backward paths are synchronized. The required number of memory bits and of control signal gates becomes \( m \) times as compared to the case of the serial PCM switching. These are summarized in the second column of Table 2(a). The required number of components when the forward and the backward paths are not synchronized is shown in the second column of Table 2(b).

### 3-3 JUNCTOR GATES FOR PARALLEL PCM SWITCHING

The configuration for the parallel PCM switching is similar to that for the serial PCM switching except for the fact that the speech path gates becomes \( b \) times for parallel transmission and that the memory capacity to store control information becomes \( b \) times because of the increased time-division multiplexity. Fig. 8 shows the memories and gates for the purpose are doubled as shown in the first column of Table 2(b).

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#### Table 1 (a) REQUIRED NUMBER OF GATE AND MEMORY ELEMENTS FOR A PAIR OF PULSE SHIFTERS CONNECTED TO A PAIR OF TRUNKS WHEN THE PULSE SHIFTER PAIR IS SYNCHRONIZED

<table>
<thead>
<tr>
<th>Component</th>
<th>Serial PCM</th>
<th>Bit Interleaved PCM</th>
<th>Parallel PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory total</td>
<td>( 2(2m-k) )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Control Signal</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Memory total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
</tbody>
</table>

#### Table 1 (b) REQUIRED NUMBER OF GATE AND MEMORY ELEMENTS FOR A PAIR OF PULSE SHIFTERS CONNECTED TO A PAIR OF TRUNKS WHEN THE PULSE SHIFTER PAIR IS UNSYNCHRONIZED

<table>
<thead>
<tr>
<th>Component</th>
<th>Serial PCM</th>
<th>Bit Interleaved PCM</th>
<th>Parallel PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory total</td>
<td>( 2(2m-k) )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Control Signal</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Memory total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
</tbody>
</table>

#### Table 2 (a) REQUIRED NUMBER OF GATE AND MEMORY ELEMENTS FOR A PAIR OF JUNCTOR GATE GROUPS CONNECTING A JUNCTOR PAIR TO A JUNCTOR PAIR WHEN THE JUNCTOR GATE PAIR IS SYNCHRONIZED

<table>
<thead>
<tr>
<th>Component</th>
<th>Serial PCM</th>
<th>Bit Interleaved PCM</th>
<th>Parallel PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory total</td>
<td>( 2(2m-k) )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Control Signal</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Memory total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
<tr>
<td>Gate total</td>
<td>( 2m )</td>
<td>( 2m )</td>
<td>( 2m )</td>
</tr>
</tbody>
</table>
the configuration when the forward and the backward paths are synchronized. The required numbers of components when the forward and the backward paths are synchronized and are not synchronized are shown in the third columns of Table 2(a) and 2(b) respectively.

<table>
<thead>
<tr>
<th>gate selector</th>
<th>serial PCM</th>
<th>bit interleaved PCM</th>
<th>parallel PCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td></td>
</tr>
<tr>
<td>control signal store</td>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td></td>
</tr>
<tr>
<td>speech path gate</td>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td></td>
</tr>
<tr>
<td>decoder gate</td>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td></td>
</tr>
<tr>
<td>transfer gate</td>
<td>2 \log_2 (k+1)</td>
<td>2 \log_2 (k+1)</td>
<td></td>
</tr>
</tbody>
</table>

TABLE 2(b) REQUIRED NUMBER OF GATE AND MEMORY ELEMENTS FOR A PAIR OF JUNCTOR GATE GROUPS CONNECTING A JUNCTOR PAIR TO A JUNCTOR PAIR WHEN THE JUNCTOR GATE PAIR IS UNSYNCHRONIZED.

4. CONFIGURATION OF SWITCHING NETWORKS

PCM switching networks generally made up of a plurality of switching stages, of which at least one should consists of pulse shifters in a toll switching systems. Denoting a stage consists of pulse shifters by M and gate consists of junctor gates by G, the type of network may be categorized by such symbolic notation as M-G2, G1-M-G1, M-G1-M-G-M etc. The number that follows the character G indicates the number of junctor gate stages. For example M-G2-M represents the network having two junctor gate stages forming a two-stage link system plus pulse shifter stages at its input and output. The networks symbolically represented by G-M-G, G-G-M-G, M-G-M, G-M-G, M-G-M-G-M etc. are symmetrical with respect to its input and output so that the networks for forward and backward connections are identical. Whereas M-G types of networks are symmetrical so that the network for forward connection consists of a pulse shifter stage followed by junctor gate stages and that the network for backward connection consists of junctor gate stages followed by a pulse shifter stage. The parallel PCM switching requires such configuration as is typically represented by M-G-M that has pulse shifters at its input and output which also perform serial to parallel and parallel to serial conversion. The serial PCM switching and the bit interleaved PCM switching both have no restriction of this sort on the network configuration.

Among the large variety of network types, preliminary studies indicated the M-G2 and G1-M-G1 types of networks were economically prospective for the serial PCM switching and the bit interleaved switching and that M-G1-M and M-G2-M types of networks were preferable for the parallel PCM switching. The subject to the present study has therefore been concentrated on these types of networks. The networks under study are for use in large-scale toll switching offices which handle traffic up to several thousand Erlangs. The scale of the networks are therefore chosen such that the number of PCM trunking (R) is from 128 to 1024 and the number of channels per frame (n) is 32 to 512.

The cost of the individual network may be evaluated in terms of the total number of memory bits and of gates required for the forward path, the backward path and their control. Introducing a parameter \( \delta \) which is the cost ratio between a gate and a memory bit, the total number of memory bits and of gates may be combined together as the total cost of the network normalized by the cost of a memory bit. The normalized total cost may further be normalized by the network scale in terms of \( R_n \), that is the product of the number of trunks and the time-division multiplexity, for comparison of the variety of networks types and scale. The cost normalized in this way may be interpreted as the relative cost per forward-backward connection and will be used as the objective function for the optimization procedure to be described in Section 5. Taking into account of the current trends in integrated circuit technology, the value of \( \delta \) is assumed to be from 1 to 5.

The constraint for the optimization procedure is the blocking probability, the approximate value of which is obtained by the probability linear graph approach assuming the binomial distribution in all switching stages. It is further assumed that \( T \) outgoing PCM trunks are available to each destination, that each of these outgoing PCM trunks are connected to an outlet of \( T \) matrices in the final junctor gate stage and that an outgoing PCM trunk is chosen out of \( T \) outgoing PCM trunks to the specified destination by open link selection. The value of the overall blocking probability is assumed to be maintained below 1%.

4.1 M-G TYPE OF NETWORKS

Fig. 9(a) shows the configuration for forward connection of M-G type of network with two junctor gate stages. The pulse shifters are provided to each of the incoming trunks. For backward connection, similar network is required that has the pulse shifters to each of the outgoing trunks instead of the incoming trunks. The M-G type of network is applicable to either the serial PCM switching or the bit interleaved switching. Fig. 9(b) shows the principle of network control. The output timing of the pulse shifter in the forward network is synchronized to the input timing of the pulse shifter in the backward network so that the pulse shifters in pair can be controlled commonly by a pulse shifter control and that the junctor gates in pair can be controlled commonly by a junctor gate control.

The junctor gates are arranged in a two stage link system. The first stage consists of \( k_1 \) matrices each with \( k_1 + 1 \) \((=R/k_1)\) inlets and \( k_1 \) outlets. The second stage consists of \( k_2 \) matrices each with \( k_2 + 1 \) inlets and \( k_2 \) outlets. The inlets of the first stage matrices and the outlets of the second stage matrices are connected to the incoming trunks and the outgoing trunks respectively. The outlets of the first stage matrices and the inlets of the second stage matrices are connected by links with the multiplexity of \( L \). The expansion rate of the network, denoted by \( x \), is given as follows.

\[
x = \frac{k_1 k_2}{L} \quad (1)
\]

For a toll switching network in which the average trunk loading is quite high, the value of \( x \) should be chosen to be greater than 1. Since

\[
R = k_1 k_2 \quad (2)
\]

\(k_1\) and \(k_2\) are given as follows

\[
k_1 = \sqrt{\frac{R}{x}} \quad k_2 = \sqrt{\frac{R}{x}} \quad (3)
\]

The cost per forward-backward connection for the serial PCM switching is evaluated as follows. For a pair of pulse shifters and a pulse shifter control, the required number of memory bits \( M_p \) and of gates \( G_p \) per forward-backward connection are respectively given from Table 1(a) by the following equations.

\[
M_p = \frac{2b}{n} (2m-1) + \left(1 + \frac{1}{n}\right) \log_2 (m+1) \quad (4)
\]

\[
G_p = \frac{5m}{n} \frac{1}{n} \log_2 (m+1) \quad (5)
\]

For the junctor gates and their control, noting that the each of the two stages connects either an incoming or an outgoing trunk to \( k_1 = \sqrt{R/x} \) links, the required number of memory bits and of gates per forward-backward connection are respectively given from Table 2(a) by the following equations.

\[
M_e = 2 \left(1 + \frac{1}{n}\right) \log_2 (\sqrt{R/x} + 1) \quad (6)
\]

\[
G_e = 6\sqrt{R/x} + 2 \left(1 + \frac{1}{n}\right) \log_2 (\sqrt{R/x} + 1) \quad (7)
\]
The numbers of memory bits and gates for the pulse shifters and the junctor gates of the bit interleaved G-M-G type of network form a G-M-G type of network. Fig. 9(c) shows the probability linear graph for the M-G type of networks with two junctor gate stages. The average loading of the input junctor gate at the input of the forward network and that at the input of the backward network can be controlled commonly, but the junctor output of the forward network and that at the input of the backward network cannot be controlled separately.

The required numbers of memory bits and gates for the pulse shifters and the junctor gates of the bit interleaved G-M-G type of network are obtained as follows.

The approximate blocking probability of a G-M-G type network with two junctor gate stages is given from the probability linear graph shown in Fig. 10(c). In the figure, $a_1$ and $a_2$ are the average loading of a junctor and an output trunk respectively. Since the network has expansion at its input which consists of the common control of the output pulse shifter of the forward network and the input pulse shifter of the backward network, the blocking probability may be evaluated by the time congestion probability as follows.

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The approximate blocking probability of a G-M-G type network with two junctor gate stages is given from the probability linear graph shown in Fig. 10(c). In the figure, $a_1$ and $a_2$ are the average loading of a junctor and an output trunk respectively. Since the network has expansion at its input which consists of the common control of the output pulse shifter of the forward network and the input pulse shifter of the backward network, the blocking probability may be evaluated by the time congestion probability as follows.
The blocking probability is given as

\[ B = \frac{b}{m} \left[ \frac{b}{m} \right] \left( 1 - a_1 \right)^a \left( \alpha_2 + a_2 \right)^{a_2} \left( a_3 + a_3 \right)^{a_3} \]

where

\[ a_1 = \frac{r}{b} a, \quad a_2 = a_1, \quad a_3 = a \]  

and \( a \) is the average trunk loading.

Single junctor gate stage may be sufficient in some cases. The cost of the pulse shifters for such a network remains the same but the cost for the gates is given by

\[ C_{\text{g}} = \frac{1}{m} \left( 1 + \frac{2b}{m} \right) \sqrt{R_x/r} + \frac{2}{ rn} \left( \log_2 \left( \sqrt{R_x/r} + 1 \right) \right) \]

Total network cost is obtained from the above equations.

The approximate blocking probability for closed link selection including external blocking is given by the probability linear graph shown in Fig. 11(c).

\[ B = \frac{b}{m} \left[ \frac{b}{m} \right] \left( 1 - a_1 \right)^a \left( \alpha_2 + a_2 \right)^{a_2} \left( a_3 + a_3 \right)^{a_3} + \left( 1 - \left( \alpha_2 + a_2 \right)^{a_2} \right)^a \]

where

\[ a_1 = \frac{r}{b} a, \quad a_2 = a_1, \quad a_3 = a \]

And the blocking probability is given as

\[ B = \frac{b}{m} \left[ \frac{b}{m} \right] \left( 1 - a_1 \right)^a \left( \alpha_2 + a_2 \right)^{a_2} \left( a_3 + a_3 \right)^{a_3} \]

where

\[ a_1 = \frac{r}{b} a, \quad a_2 = a_1, \quad a_3 = a \]

5. NETWORK OPTIMIZATION AND RESULTS

Optimum values of the network parameters \( I \) and \( x \) or \( r \) that minimize the cost of the respective types of networks with various values of \( R, m, T \) and \( \delta \) have been sought while maintaining the overall blocking probabilities below 1%. Hill climbing method has been employed for the optimization procedure in which optimum values of \( x \) has been obtained by assigning various integer values to \( I \) and \( r \) and then optimum combination of \( I, r \) and \( x \) has been chosen which give the lowest network cost. To avoid excess congestion by over-loaded traffic, the value of \( x \) is restricted to be more than 1. The cost of the network varies with the value of \( m \) and are minimum for certain value of \( m \). In the cases of the serial PCM switching and the bit interleaved PCM switching the minimum cost is obtained when \( m=16 \) for M-G2 type networks and \( m=8 \) for G1-M-G1 type of networks. And the cost of parallel PCM switching is minimum when \( m=4 \) for M-G2-M and M-G1-M types of networks. The cost of the networks is evaluated for the values of \( m \) which give the minimum cost.

Fig. 13(a) and (b) show the cost of these networks with respect to the number of trunks \( R \) for \( \delta = 3 \) and 5. Generally the serial PCM M-G2 type of networks are the least expensive for smaller values of \( R \) and parallel PCM M-G2-M type of networks are the least expensive for larger values of \( R \). The major reason for the higher cost of the bit interleaved PCM switching is that the gate selectors and the transfer gates require memories and gates \( m \) times more than that are required in the other cases. For more detailed cost comparison however, such fact should be taken into account that the required operating speed of the gate selector memories.

Figs. 12(a) and (b) summarize some results of cost comparison on optimized networks of various types against the time division multiplexity \( n \) when the gate-memory cost ratio \( \delta \) is 3 and 5 respectively. The values of \( b, R, \) and \( T \) are chosen in these figures as \( 8, 512 \) and \( 4 \) respectively.
and the transfer gates in m times slower than that of the other cases so that actual cost may be lower than what has been estimated.

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TABLE 3 OPTIMALLY DESIGNED NETWORK PARAMETERS FOR VARIOUS TYPES OF NETWORKS WHEN n=128, T=4, k=8 AND δ=3

Table 3 summarizes the optimum values of the network parameters m, l, x, k1, k2, r and R for the serial PCM, the bit interleaved PCM and the parallel PCM switching networks which give the lowest cost. The number of trunks R is chosen close to 256, 512 and 1024 although it somewhat deviates from these values due to the fact that k1, k2 and l take integer values only.

6. CONCLUSION

Optimum design of three major categories of PCM switching networks all with partial access pulse shifters has been explored for application to large-scale toll offices capable of handling several ten thousand Erlangs. The optimization is performed taking the overall blocking probability as the constraint and the relative cost of the required memories and gates as the objective function. The cost of gates are interpreted to the cost of memories by means of a parameter, the gate-memory cost ratio, under the approximation that the cost of memories or gates are independent to the operating speed or device layout.

The comparison between optimized networks indicates that for networks having larger time-division multiplexity and smaller number of time-division trunks, serial PCM M-G type of networks with two junctor gate stages are the most economical and that for the network having smaller time-division multiplexity and larger number of time-division trunks, parallel PCM M-G-M type of networks with two junctor gate stages are the most economical. It is also known that the difference in cost of the optimized networks of three categories are not quite significant as intuitively expected. The difference may be overcome by further improving the network configuration, by the progress of solid state circuit technology or by more detailed evaluation of component cost.

REFERENCES

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