ABSTRACT

Digital switching equipment provides numerous subjects of investigation for traffic theorists. The traditional topics of dimensioning and forecasting remain, but, additionally, efforts must be addressed to the delays introduced into the signal by buffering, regeneration, and time slot alignments within the matrix. Also, points of measurement must be developed for the collection of traffic and other administrative data. The complexity of the hardware and the control software can be reduced enormously if a new and different telephone set is designed to accommodate digital transmission and new electronic technology.

BACKGROUND INFORMATION

The national toll network in the United States employs five levels of switching equipment, identified as Classes 1 through 5. The first four classes are trunk switches; all of which are identified as Class 5 equipment, or by PABX's which in turn are served by Class 5 exchanges. Other terms apply in other countries, but the comments found below are applicable to the local subscriber switching equipment whatever its name might be.

A number of digital Class 5 systems now are in service in the United States and the trend is increasing there as well as elsewhere. Planners now speak of the situation "when the whole world is digital", recognizing that the circumstance probably will not prevail within this century. Most of these digital switches employ pulse code modulation (pcm) but other modulation schemes exist or are under discussion. Regardless of the coding architecture, digital switches at any level introduce new traffic dependent phenomena, and the Class 5 environment in particular is susceptible to several lineaments not found in analog space division equipment. Some of these will be described here, however, no attempt is made to offer solutions. Instead, it is the intent that several potential problems be identified for investigation before these are revealed by digital switching equipment in actual service.

In the past, traffic theory has catered to the basic concerns of how much equipment is needed and when. These problems of dimensioning and forecasting will remain, but the traffic theorist now must solve other parametric problems which relate to the quality of the digital switch as a signal processor. For example, little attention has been granted to such things as the delay of signals and intelligence which is caused by the switch design, nor of the effects that delay can have upon the patting arrangements.

DELAY

GENERAL COMMENTS

The effects of delay are rather insidious, raising difficulties in the control of echo, and with other subjective evaluations of transmission quality. Without exploring these effects in detail, it is sufficient to state that any switch—digital or analog—should introduce as little delay as possible to the electrical signals which traverse its boundaries. It should be noted that worldwide the standard frame (sampling) rate for pcm is 8000 per second. (An 8-bit code also is standard, but almost nothing else is). Should some vagary of the digital switch design cause the intelligence to be delayed by just one frame (or by 1/8000 second), this is the equivalency of increasing the length of the transmission path by as much as 37 km if derived by electromagnetic radiation, and in no case less than about two km for inductively loaded cables. Although a single such event is of no particular concern for most voice communications of nominal distances, an accumulation of these effects can be bothersome on long haul voice circuits and for some types of data communications.

BUFFERING

An important feature of an integrated network of digital switches and transmission facilities is that all segments and components are synchronized by a master clock system. Several master clocks must exist to service a country of large geographical size (such as Australia, the Soviet Union, and the United States), and of course, most countries will choose to furnish the master clock for its own network. It follows that many master clocks will exist.

Given that even two master clocks are in service, the problem arises immediately that the rate of each clock will differ from the others so that some switches will service circuit groups which have been timed by two or more clocks. Even when exposed to only one clock, a switching control will find that the frames arriving on various trunks will not be aligned. This is shown in Fig. 1, where the switch at Node 2 receives its timing information according to the conditions at "a". Within Switch 2, it is convenient to slip the framing by the small interval S. The circuits from 1 to 2 are synchronized by the shorter path MC-1 and this timing information is conveyed to Switch 2 by the path 1-2 according to pattern "b", causing a misalignment within the switch at Node 2 by the amount shown. For similar reasons, the timing of circuits from 3 to 2 also differ as indicated.

![Fig. 1](image)

The switch at 2 must receive each circuit into an incoming buffer so that slot one of all circuits can be aligned while within the confines of the switch. As a general premise, the rule of "early must wait for late" applies in buffering. As an example, if slot one within the switch has just passed and if a trunk now presents slot one of a new frame, this entire frame must be delayed until slot one again appears within the switch. Thus,
the digital code group will experience a delay of as much as \( N-1 \) time slots because of buffering, where \( N \) is the number of slots within a frame. Regardless of the number of time slots available, \( N \) slots of slip represents 1/8000 second.

If the switch accommodates circuit groups which are timed by different master clocks, then the minute differences in clock rates ultimately will cause synchronization slips when connections are made between two of these groups. These slips will cause a bit to be missed completely when a circuit timed by a slow clock is transmitting into a fast, or will cause the same bit to be sent twice for fast into slow.

Undoubtedly, the traffic disciplines will be asked to study, or at least be aware of the effects of buffering and of master clocks which differ in rate.

**REGENERATION**

Although buffering aligns all frames as these enter the depths of the switch, other considerations make it difficult to maintain the alignment of time slots once inside. Some of these result from the need to regenerate the pulse stream at regular intervals. For example, Fig. 2 depicts a series of clock pulses at an incoming stream of bits which is to be regenerated. The regenerator will inspect each bit location and decide whether a zero or one is present and then recreate the same element at its output terminals. It can be seen that even an ideal regenerator inserts an inherent delay of about one half a bit. Similar comments apply if an 8-bit character merely is parked momentarily prior to being transported elsewhere in parallel. A number of regenerations or transportations occur within the typical switch so that several half-bit delays are introduced into the digital stream.

Should it occur that various path assignments involve differing amounts of transportation and regeneration, then delay will not be uniform from connection to connection. This will be of particular concern if the internal path arrangements are changed during a connection. These conditions are discussed next.

**DELAYS CAUSED BY PATH MARKING**

The teletraffic society is aware that the digital switch employs a protocol of time slots to effect transmission paths within the matrix. Also, all practitioners of the art know that the digital switch matrix can be transformed into a space division configuration that is equivalent in topology and connectivity. Figs. 3 through 5 show several of these conversions, however, none of these diagrams reveal that a time delay is introduced into the signal as it traverses the matrix, and further, that this delay may be dependent upon (a) the particular traffic state which exists when the call is set up, or (b) the states that may occur while the call is in progress.

For example, the system shown in Fig. 6 can be implemented so that connections are effected by employing the same time slot to sample in both the input and the output groups, or (b) any slot on the left can be aligned with any slot on the right. The first example manifests the space equivalency of the three-stage link matrix of Fig. 7 whereas the second is exemplified by a three stage system of Fig. 8 (Fig. 8 is the same pathing arrangement as in a small step-by-step system with one stage of selection). In Fig. 7 the transmission delay is the same (or nearly so) between any inlet-outlet pair. Fig. 8, however, introduces a delay at the second stage which is dependent upon which left slot is being aligned with which right-hand slot. The general rules are given in Table I for a hypothetical system of five slots; others can be derived easily. It can be seen that as much as \( N - 1 \) slots of delay can be imposed by the second stage. The salient points here are (a) several such stages may exist in the same switch, and (b) the delay is not constant if the control reassigns time slots of existing connections to reduce congestion for other calls being set up.

**Fig. 2** Bit stream a) before and b) after regeneration slips the entire bit stream by approximately one half bit even in the ideal case. Practical slips may be much greater.

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**In such schemes, several code groups are switched as an entity by an appropriate path arrangement. This path then is released for reassignment to some other group, so that the next code group from the connection of interest is assigned a new and (likely) different path. The limiting case occurs when each code group of a particular connection is assigned a different path. In these designs, all cases of congestion in path assignments will cause a segment of the bit stream to vanish so that extremely low blocking rates are necessary if the switch is not to introduce an excessive amount of error. Indeed, the allowable blocking is so minute it is but a small step to nonblocking operation. Numerous unsupported claims of nonblocking have been made for digital switches, but there is nothing inherent in these systems which guarantees that congestion will not occur. The traffic theorist probably will be required to determine criteria for low and nonblocking operation both to support control disciplines that reassign paths and to determine optimum slot structures for families of switch designs.**
In more complex designs it becomes desirable to employ numerous time slots internally because more freedom exists in allowing for regeneration and transportation. Stated otherwise, if the internal architecture caters to 24 channels in a frame of 193 bits (standard T-1 format as used in the United States), and if each manipulation involves two bits of delay, then the system cannot handle the bit stream more than about 96 times internally, if the total delay is to be one frame or less. If 96 channels were used internally in a frame of 789 bits (standard T-2, 4 x 193 = 772 + 17 "stuffed" bits) then about 344 manipulations become feasible. Thus, the designer views additional time slots not only as paths, but the digital stream. (The slips and delay specifications quoted here are for illustrative purposes only and probably bear no relationship to an actual equipment.) In any event, the traffic theorist may be asked to evaluate the optimum number of internal time slots when considering simultaneously the effects of path reassignment, regeneration and slipping.

![Diagram](a)

**Each Path Equivalent To One Time Slot**

**Points of Measurement**

A digital switch offers little opportunity to obtain traffic data unless the need is recognized early in the design stage. In particular, most existing designs present almost no electrical points where leads could be attached to accommodate traffic measurement equipment that might become desirable. The administrations will state the need in the form of performance requirements imposed upon the manufacturers and these in turn must be transformed into measurement methods and data reduction techniques which can be accommodated by the switch designers. Of course, the traffic specialist is the proper one to perform these analyses and make proper recommendations.

**A New Telephone Set**

As noted in Reference 1, all present switch designs are burdened by the signalization format of the existing telephone set. If a new telephone instrument is adopted for digital switches, the traffic load will be reduced significantly and the software design will be simplified as well.

From a traffic viewpoint, the most significant improvement will come when the set is used to buffer the human user from control of the switch. By means of microprocessor technology in the set and digital transmission, the called number is entered completely into the set without the switching control being involved at all. Upon entering the last digit, the caller presses an "end of instructions" (EOI) button which causes the set to transmit a HAIL signal to the switching control. The switching control then requests a SPILL or DUMP, and receives the called number and other information at the basic rate of 8000 characters per second. A single station can be interrogated in about six or seven milliseconds, so that with suitable control software and processing capability, a single register could serve an exchange of many tens of thousands of lines.

If such a telephone set can be specified, the traffic theorist undoubtedly will be asked to investigate the performance of the new control architecture within the switch.

**Figure 4** Equivalent space division matrix of system shown in Fig. 3. Note that time slots are assigned permanently to lines on left side.

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Fig. 7 Link equivalency of matrix in Fig. 6. Congestion occurs unless the same time slot can be assigned to the left and right hand terminals.

Fig. 8 Space division equivalency of matrix in Fig. 6 where any slot on the left can be aligned with any on the right. This arrangement is the same as in a three-stage step-by-step system.

TABLE I
Delay (d) Introduced in Aligning Time Slots (5 slot system)

<table>
<thead>
<tr>
<th>To Slot b</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>From Slot a</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
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<td>2</td>
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<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ d = N + b - a \]

\[ N = 0, b < a \]

\[ N = 5, b < a \]

References:
1. Fleming, Paul "Traffic Considerations of a New Generation of Telephone Set", 9th ITC Madrid 1979
3. "Readings in Pulse Code Modulation" Demodulation a series of articles combined into one binding, GTE Lenkurt San Carlos, CA 94070 1973