ABSTRACT
In a first paper at this 9th ITC /8/, PCM (TDM) switching arrays having up to 6 stages and up to about 100,000 terminations, were investigated with regard to their standardized costs per termination, as a function of the cost ratio "gate to memory-bit".

In this context - the influence of the number and sequence of stages (T-Stage),
- the degree of multiplexing (30, 120 time slots per multiplex line)
were considered. Furthermore, new PCM-Charts for the quick design of economic PCM switching arrays were developed.

This second paper completes these studies by comparisons between PCM switching arrays and their equivalent SDM switching arrays. Handy formulae for the best possible economic design of PCM and SDM arrays, resp., are presented and derived.

The loss versus the carried traffic of PCM arrays, having S=3 up to 6 stages and with M=30 and 120 time slots per highway are compared with each other and with equivalent SDM link systems.

Furthermore, the relative costs per termination are calculated for these PCM and SDM array-structures and drawn versus the size of these arrays.

1. INTRODUCTION
As mentioned in the abstract, this paper completes the extensive PCM array investigations in /8/. The rapid decrease of costs for digital switching components makes it worthwhile to compare SDM and PCM switching arrays with each other. As a basis of such comparisons both, PCM switching arrays as well as their equivalent SDM switching arrays, have to be designed optimally, i.e. as cost saving as possible.

Chapter 2 presents two different sets (No.1 and No.2) of design formulae for "optimal" SDM and PCM switching arrays respectively, basing on two different boundary conditions.

In Chapter 3, the traffic behaviour, i.e. the point-to-point loss B_{PP} versus the carried traffic per termination is discussed for such least-cost PCM and equivalent SDM structures.

In Chapter 4, the standardized costs per termination (CPT) are considered under various assumptions for the costs of metallic 4-wire crosspoints on the one side and for gates and memory-bits on the other side. They are calculated for switching arrays having S=3 to 6 stages and up to about 100,000 terminations. A traffic of 0.8 Erl/terminal and a point-to-point loss of 0.1% are fixed parameters of these graphs.

In Chapter 5, the design formulae of type 1 and type 2 are derived for both, SDM and PCM arrays.

2. FORMULAE FOR THE COST SAVING DESIGN OF SDM AND PCM SWITCHING ARRAYS

2.1 General Remarks
The formulae being discussed in this chapter and being derived in the annex, hold for the structural parameters of switching arrays in case of any operation modes, namely
a) 2-sided systems,
b) 4-wire arrays with unidirectional or bidirectional traffic flow;
c) 4-wire arrays with "combined" switching (PCM or SDM) of bidirectional traffic through one unidirectionally operated array.

As far as the expression "termination" is used, note that one termination includes in case of 4-wire switching always both speech directions which belong to one speech connection (cf. /7/).

In deriving such formulae for least-cost switching array structures, this paper starts from two different boundary conditions. This holds for SDM arrays as well as for PCM (TDM) arrays. The basic idea of these two boundary conditions (named No.1 and No.2) shall first be explained briefly by means of a symmetrical two-sided SDM link system.

Another two methods for the structural design of "crosspoint minimal" switching arrays are mentioned in Chapters 2.8 and 2.9. The reasons, why their application is not suitable here, are explained.

2.2 Boundary Condition No.1
Be designed a two-sided link system having S stages and N outlets per side (i.e. = 2 N terminations). Furthermore, a "single linkage" (SL) structure is desired (cf. Fig. 2.1. Chapter 5.1). Condition No.1 prescribes for SDM arrays that the desired crosspoint saving structure has the smallest possible requirement of crosspoints per line (trunk, inlet, resp.).

\[
\text{CPL} = k_1 \cdot B(k_2 + k_4 + \ldots + k_8) = k_1 \cdot B \cdot \sum_{i=2}^{8} k_i
\]

where \( B = \frac{1}{T} \cdot \frac{1}{S} \) means the "expansion factor" of the multiples \( \{k_i\} \) in stage No.1.

Hereby the transparency function

\[
T = \frac{S-1}{N} \sum_{j=1}^{S-1} k_j \cdot \left(1 - \frac{j}{S}ight) \cdot k_S
\]

is assumed to have a constant value, as a boundary condition for the derivation of the design formulae. In Eq. (2) \( k_j \) means the number of outlets per multiple in the stages No. 1, 2, 4, 8; \( S \) and \( S_{+1} \) denotes the carried traffic per link from a stage No.j to No. (j+1).

The design formulae derived with this boundary condition have already been applied in /2/ as well as for the "NIK-Charts" /5/. They allow the quick design of crosspoint saving SDM link systems. These formulae are listed in Table A (part SDM 1). As to the derivation see Chapter 5. More details can be found in /7/.

2.3 Boundary Condition No.2
Condition No.2 for SDM switching arrays does not use the "transparency condition" according to Eq. (2). Instead, one starts from the desired number N of inlets (outlets) per side. Regarding the above mentioned condition of a "single-linkage structure" (SL) these N inlets per side can be accessed from "the midst" of the symmetrical switching array (cf. Fig. 2.1). If

\[
N = \sum_{j=1}^{S_{+1}} i_j
\]

The notation \( S_{+1} \) means the next lower integer value. E.g. for \( S=4 \) as well as for \( S=5 \), it holds \( S_{+1} = 3 \).

The design formulae basing on this boundary condition No.2 are listed in Table A, part SDM 2. As to the derivation, see Chapter 5.
2.4 Example for the Use of the Formulae Sets

Table A:  

<table>
<thead>
<tr>
<th></th>
<th>SOM 1</th>
<th>SOM 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>S=2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>i,j</td>
<td>g1=64</td>
<td>g2=128</td>
</tr>
<tr>
<td>j=1</td>
<td>g3=128</td>
<td>g4=64</td>
</tr>
<tr>
<td>k1</td>
<td>k2</td>
<td>k3</td>
</tr>
<tr>
<td>k1</td>
<td>0</td>
<td>k2</td>
</tr>
<tr>
<td>k2</td>
<td>1</td>
<td>k3</td>
</tr>
<tr>
<td>k3</td>
<td>0</td>
<td>k4</td>
</tr>
<tr>
<td>k4</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

N = 512  

Fig. 2.1a: Four Stage Array, Mode SDM 1

Fig. 2.1b: Four Stage Array, Mode SDM 2

2.5 Boundary Conditions No.1 and No.2 Applied to PCM Switching Arrays

Here only the structure of the multiplex link lines within a PCM switching array need be considered and not the structure of the individual link paths as in a SDM link system.

According to the same basic ideas as for SDM 1 and SDM 2, one obtains the formulae sets PCM1 and PCM2, respectively, for gate minimal arrays. In contrast to SDM switching systems one has to distinguish here between switching arrays of various sequences of time and space stages.

Table B contains the formulae for the design modes PCM 1 and PCM 2. The methods PCM 1 and PCM 2 differ only in case of switching arrays with more than 2 space stages.

As to the derivation, see Chapters 5.3 and 5.5.
2.6 Examples for the Use of Design Modes PCM 1 and PCM 2

2.6.1 Five-Stage TSSST PCM Array

Fig. 2.3 shows two 5-stage PCM switching arrays of the type TSSST with \( N=500 \). The array in Fig. 2.3 is designed according to Mode PCM 1. The values in parenthesis hold for the design according to Mode PCM 2.

For both arrays, the design modes consider here only the 3-space stages in the middle and their matrices.

The mode PCM 1 yields, for 49 multiplex lines (ML) per side of the array, uniform matrices with \( h_2=j_2=j_3=h_4=j_4=7 \). These 49 MLs correspond to 1470 speech paths. The mode PCM 2 yields two different matrix sizes, namely \( h_2=j_2=h_4=j_4=5 \) and \( h_3=j_3=10 \). Therewith 50 MLs are connected to the TSIs of the T-Stages on both sides.

It should be focused upon the fact that an expansion between inlets and outlets of the first stage (and a corresponding concentration in the last stage) is performed in both cases only by increasing the number of "internal time slots" per internal multiplex line (ML). The number of MLs and the size of the matrices remains constant.

2.6.2 Six-Stage TSSST Array

As a further example, a 6-stage array is considered. It is designed according to the two modes PCM 1 and PCM 2, respectively.

Here 125 and 108 highways, resp., were chosen, leading to optimal, i.e. gate minimizing arrays (see Fig. 2.5, a, b).

The diagram, being analogous to Fig. 2.4, is presented in Fig. 2.6. Here too, the necessary expansion \( \beta \) is greater for the PCM array designed according to mode PCM 2. Its resulting relative costs per termination are slightly smaller in this case.

Regarding the small differences of costs, as well as the advantage of uniform matrices in all space stages, the following chapters will consider only switching arrays being designed according to mode PCM 1 and PCM 1, resp.
1.6
EXPANSION FACTOR $\beta$

1.4

B$_{pp}$=0.1%

1.2

B$_{pp}$=1%

1

0.8

0.6

0.4

0.5

0.6

0.7

0.8

0.9
carried traffic per termination / Erl

TSSSST

Fig. 2.6: Comparison of the Relative Costs for the TSSSST Array, Mode PCM 1, PCM 2

0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.2 1.4 1.6

20 30 40 50 60 70

Costs per termination / Bit

PCM 1

PCM 2

2.8 Overall Cost Optimization of PCM Switching Arrays

A further method for designing an "optimal" PCM switching array is to minimize the costs of gates and speech memories and the respective control memories as a whole. This can be done by differentiating the overall cost formula of a PCM switching array, with respect to the inlets and outlets of the space switches. Also, this principle is applicable for PCM arrays having 3 and more space stages (like method PCM 2). The design for arrays with less than 3 space stages is already determined by the demand of a symmetrical structure.

This overall cost optimization was applied to all PCM arrays having $>2$ space stages. Here, the minimum costs depend on the size of the space switches and their respective control memories; the number of the time-slot interchanges of the T-Stages has no influence.

The result is, that the difference of the costs between only gate minimal arrays and overall least-cost arrays is negligible.

There are two reasons:

First: Strictly optimal values for the size of the space switches and the control memories can normally not be observed, because only integer values of inlets $h$ and outlets $j$ can be realized. The same holds for the memory bits per storage place. Therefore, the practical realization is generally more expensive than the theoretical cost minimum.

Second: Overall cost minimization generally yields smaller space switches in the first S-Stage than even the gate minimal solution (mode 2). As a rule, the expansion factor therefore has to be remarkably increased in order to achieve a prescribed high grade of service. Consequently, the costs increase and the desired savings may again be compensated.

Overall cost minimization has been checked for many PCM arrays. The result was always as described above. Therefore, this third optimization principle will not be applied.

2.9 The Optimum Link (CPE-) Method /1/.

This method for the structural design of SDM link systems yields the utmost minimum requirement of crosspoints per Erlang for SDM link systems with prescribed transparency $T$ according to Eq. (2). However, the condition of a "single linkage" (SL-) structure as required here, cannot be observed. (Detail are discussed in /7/).
Fig. 3.1-3.4: Point-to-Point Loss Versus the Carried Traffic per Termination for PCM and Equivalent SDM Arrays
3. LOSS VERSUS CARRIED TRAFFIC

3.1 General Remarks

In this chapter PCM switching arrays of the types TST, TSSS, TSSST, SRTS and TSSST are considered. The loss $B_{PP}$ versus the carried traffic per inlet is drawn for PCM arrays being designed according to the mode PCM 1 and assuming $M=30$ or 120 time slots per multiplex line (ML). Furthermore, equivalent SDM systems being designed according to mode SDM 1 with a minimum requirement of crosspoints per termination are presented. Interleaved wiring is applied for SDM arrays having $S > 4$ stages. The selected arrays consider smaller systems with $S=3$ stages, medium ones with $S=4$ and larger ones with $S=5$, 6 stages.

For all examples the characteristic traffic per inlet is assumed to be 0.8 Erl. All arrays were expanded individually such that a point-to-point loss probability (one attempt only) in the range of $E=0.1\%$ was achieved. The loss curves have been checked by simulation runs.

3.2 Results

The loss differences between equivalent SDM and PCM arrays result only from two reasons:

a) The necessity to have an integer number of inlets/outlets per stage,

b) the different sizes of the first stage multiples cause different link loads for a certain loss. The higher the link load is, the steeper is the increase of loss.

This is evident for all $T_{...,T}$ arrays, with $M=120$ time slots per multiplex line. They have the steepest increase of loss because the internal TS carries a higher traffic load (Figs. 3.1, 3.2, 3.3, 3.5). This means that the sensitivity against overload is greater. On the other hand, a solution with $M=120$ time slots per ML will often be cheaper (cf. Chapter 4).

In Fig. 3.4 the SDM array has larger first stage multiples than the corresponding PCM arrays (SSST). Consequently, this SDM array has the better link efficiency and therefore, the steepest increase of loss versus the carried traffic.

In Fig. 3.3 the curves for SDM arrays are shown having a first stage expansion of $1519$ and $1520$, respectively. The desired point $0.8/0.15$ lies in between. The same holds for the curves (2a) and (2b) in Fig. 3.5, where the two SDM systems have an expansion $914$ and $915$, respectively.

4. COSTS PER TERMINATION

4.1 General Remarks

The diagrams in Figs. 4.1 to 4.6 show the (standardized) costs per termination (CPT) for SDM and PCM switching arrays. Both types have a carried traffic $Y/N=0.8$ Erl, per termination and a point-to-point loss $B_{PP}=0.1\%$ (one attempt) as fixed diagram parameters. The curves for the PCM arrays base on a cost ratio "gate to memory-bit" of 0.8. One cent (U.S. currency) per memory-bit can be assumed to be a reasonable price for the time being, if the costs for the control of the memories are included.

For SDM 4-wire systems the costs per 4-wire crosspoint are assumed to lie between $71$ and $85$ (U.S. currency), i.e. a relative price of about 100 to 500 compared with 1 memory-bit. If, e.g., 30 crosspoints per termination were required, with a cost of $52$ each, the diagram would show standardized costs of 6000 per termination.

Regarding this very high price relation between metallic crosspoints and memory-bits, one has to consider that PCM systems cause a lot of additional costs per termination which cannot simply be included into these diagrams!

These additional costs result among others from higher peripheral costs, such as the BORSHT functions, the CODEC's etc.

4.2 Results

The 6 diagrams deal with the following PCM array types: TST, TSST, TSSS, TSSST, SRTST and TSSSTT. They show the relative costs per termination (CPT) in the unit "bit" versus the number $N$ of terminations of the system ($N=600 \ldots 20,000 \ldots 100,000$). In all diagrams the least cost SDM arrays base on a price per metallic crosspoint of 100, 250, 500 bits (see curves No.1,2,3).

The significant results of Figs. 4.1 to 4.6 can be summarized as follows:

a) In any case PCM switching arrays have much lower costs per termination than SDM switching arrays.

b) Switching with $M=120$ TS per ML instead of $M=30$ TS (i.e. serially with 80 bit/sec.) leads to a decrease of CPT of about 10 to 30% referred to the pure switching array costs.

c) The compared SDM switching arrays show a significant increase of CPT as the number of stages increases.

d) PCM arrays having 3 stages compete with arrays having $S > 4$ stages as long as the number of terminations does not exceed $N=3000$ (with $M=30$). Using $M=120$ TS per ML 3-stage arrays up to at least 20 000 terminations may still be economic.

e) PCM arrays with 4 to 6 stages do not have significantly different costs per termination. However, the complexity of path allocation and central control increases with the number of stages.

Therefore, the thumb rule for the economic design of PCM switching arrays reads:

Choose a small number of stages combined with a high number of time slots per multiplex line.
5. ANNEX

Derivation of the Design Formulae for Crosspoint or Gate
Saving SDM and PCM Switching Arrays

5.1 Prerequisites

As prerequisites for the design modes hold:
- The arrays are symmetrically structured (I)
- Expansion and the corresponding concentration are performed in the first and the last stage, resp. (II)
- The intermediate stages switch 1:1 (III)
- Only structures with "single linkage" (SL-) wiring (IV) are considered.

"SL" is defined as follows, e.g. for S=4 stages (cf. Fig. 2.1, and /9/).
\[ k_1 = g_4, k_2 = g_3, k_3 = g_2, k_4 = g_1 \]
\[ g_1 = k_2 = k_3 = k_4 \] (width of the connection graph)

In case of SL-wiring, the following formula holds for the number of lines (trunks) per side of a SDM link system
\[ N = \prod_{i=1}^{S} \frac{k_j}{i_j} \] (A1)

5.2 The Crosspoint Minimization Mode SDM 1

The derivation of the structural parameters \( i_j \) and \( k_j \) of a SDM switching array has to achieve a minimum number \( C_P L \) being defined as in Eq. (1).

The boundary condition \( T = \text{const} \) according to Eq. (2) can be simplified, because the carried traffics \( a_j \) per link \( (j = 1 \ldots (S-1)) \) are the same between all stages and independent of the size of the multiples (see prerequisite III). Hence, Eq. (2) can be replaced by the product
\[ P = \prod_{j=1}^{S} k_j \] with \( k_1 = \frac{P}{\prod_{j=2}^{S} k_j} \) (A2)

and be used as boundary condition. Therewith the partial derivation of \( C_P L \) with respect to \( k_j \) yields \((j=2 \ldots S)\)
The boundary condition for this mode is the prescribed number of lines (trunks) \(N\) to be connected per side of a SDM link system and observing the prerequisite IV. As an example the derivation is shown for \(N=4\) stages. It holds

\[
N = n_1 \cdot 2^2 \cdot 3 = k_2 \cdot k_3 \cdot k_4 \quad \text{see Fig.2.1.b) (A11)}
\]

\[
\text{DCPL} = -\frac{p}{k_j} \sum_{j=2}^{S} \frac{1}{k_j} + \beta = 0
\]

From this follows, \(k_j = \frac{p}{\sum_{j=2}^{S} \frac{1}{k_j}}\), \(j = 2 \ldots S\) (A3)

and \(i_2 \cdot i_3 \ldots i_{S-1} \cdot k_2 \cdot k_3 \ldots k_S\) (A4)

for the assumed symmetrical structures (see prerequisite I). From the known number of HW multiplex lines per side and the internal MLs via the intermediate MLs and their space stage matrices depends on the product \(\text{GPM} = j_1 \cdot 8(j_2 \cdot j_3 \cdot j_4 \ldots j_S)\) (A7)

Again, \(j_1 = \frac{1}{h_1}\) means the expansion factor in stage No.1, if an \(S \ldots S\) array is considered, elsewhere here \(h = 1\).

Only those stages \(S\) must be included into the sum GPM which are space-stages!

The grade of access from the incoming to the outgoing external MLs via the intermediate MLs and their space stage matrices depends on the product

\[
P^* = \frac{S}{\prod_{j=1}^{S} j_1} \quad \text{and with } j_1 = \frac{p^*}{\prod_{j=2}^{S} j_1}
\]

(A8)

Only those indices No.1 (of space stages) must be regarded which contribute to this access "from left to right" or vice versa.

Be considered a constant value \(p^*\) which must be achieved with a minimum number of GPM.

The partial derivation of GPM with respect to the inlets \(j\) of all concerned space matrices leads to a uniform size

\[
j_1 = h_1
\]

(A9)

From the known number of HW multiplex lines per side and from the prerequisites III and IV follows (analogously to SDM arrays)

\[
h_1 = j_1 = \sqrt[2N+1]{\text{HW}}
\]

(A10)

\[
5.4 \text{ The Crosspoint Minimization Mode SDM 2}
\]

The boundary condition for this mode is the prescribed number of lines (trunks) \(N\) to be connected per side of a SDM link system and observing the prerequisite IV. As an example the derivation is shown for \(S=4\) stages.

It holds

\[
N = n_1 \cdot 2^2 \cdot 3 = k_2 \cdot k_3 \cdot k_4\]

(see Fig.2.1.b) (A11)

\[
\text{Eq. (A11) does not include } i_4 \text{ and } k_4, \text{ respectively.}
\]

These values follow from the symmetry condition I, i.e.

\[
k_1 = i_4, \quad i_1 = k_4
\]

(A12)

with prerequisite II

As the same prerequisites I to IV hold, one obtains with (A12) and (1)

\[
\text{CPL} = 2k_1 + \beta \cdot k_2 + \beta \cdot k_3
\]

(A13)

and with (A12) in (A11)

\[
k_1 = N-B \cdot \frac{1}{k_2} \cdot k_3
\]

(A14)

Partial derivation \(\frac{\text{CPL}}{k_j} = 0\) yields

\[
k_2 = k_3 = 2N \cdot \frac{1}{k_2} \cdot k_3
\]

(A15)

with prerequisite III follows \(i_2 \cdot k_2 = i_3 \cdot k_3\)

(A16)

with (A14), (A15) and (A12)

\[
k_2 = \frac{B}{k_3} \cdot k_1 = i_1
\]

(A17)

with (A11), (A16) and (A17)

\[
N = i_1 \cdot k_2 \cdot k_3 = i_1 \cdot 3
\]

(A18)

and hence

\[
j_1 = \sqrt[2N]{3}
\]

(A19)

with (A17)

\[
j_2 = \sqrt[2N]{3}
\]

(A20)

\[
5.5 \text{ The Gate Minimization Mode PCM 2}
\]

This mode yields formulae which correspond to those of mode SDM 2, see Table 8.

Remark: All above derivations can be found more detailed in the PCM-CHARTS / 7/.

REFERENCES:


/6/ LOTZE, A., RUDER, A., THIERER, G.: On the Point-to-Group Selection and Selection Loss in Link Systems with Symmetrical or Interleaved Link Wiring. (To be published)

/7/ LOTZE, A., ROTHMAIER, K., SCHELLER, R.: PCM-CHARTS for the Design of Economic PCM Switching Arrays. (To be published)

/8/ ROTHMAIER, K., SCHELLER, R.: Design of Economic PCM Arrays with a Prescribed Grade of Service.
