

LOW COST DESIGN MODIFICATION FOR IMPROVING REAL-TIME CAPACITY

Joe BRAND

Hitachi America, Ltd.
Norcross, Georgia, USA

A low cost design modification for significantly increasing the real-time capacity of a Stored-Program-Control (SPC) PBX is presented. The capacity increase is achieved with very little development effort and only a small increase in hardware cost. The method takes advantage of the fact that the majority of the processing involves a small fraction of the internal memory of the system. This trait is thought to be common for SPC switching systems [1].

For increasing the processor real-time capacity, two alternatives were considered. One involved increasing the processing speed (Alternative 1), and the other involved adding auxiliary processors and removing work from the central processor (Alternative 2). Using a queuing model calibrated with actual data, a capacity relationship for the central processor was determined as a function of both percent of work moved out of the central processor and percent increase in speed of the central processor. Although the idea of providing adequate capacity increase without auxiliary processors was initially met with skepticism, the model showed that either alternative would provide adequate capacity increase. The capacity increase for Alternative 1 results from three factors: (1) decreased time spent doing overhead work, (2) decreased time per call, and (3) increased allowable processor occupancy at maximum capacity. The third factor is a result of queuing theory when the capacity definition is based on maximum allowable queuing delays. Alternative 1 was chosen because it required less development effort and less hardware costs.

Advances in the microprocessor technology permitted up to a 50 percent increase in processor clock rate which suggested the alternative of increasing the real-time capacity by speeding up the processor. However, a 50 percent speed-up of the basic clock rate did not imply a 50 percent increase in effective processing speed because of the memory access speed limitation. In fact, without increasing the memory speed, only a marginal gain could be realized with a faster processor. Faster memory chips were available at lower density and higher cost. A large real-time processing capacity increase can be achieved by replacing the processor with the high-speed version and redesigning the memory boards. The redesign would involve replacing the memory chips with the high-speed, low density chips and optimizing other circuitry for speed. Because of the low density of the high speed memory devices, the

number of memory boards required becomes excessive, escalating cost and physical space beyond acceptable limits.

A real-time analysis involving laboratory measurements showed that about 70 percent of the processing time involved less than one percent of the total memory. This amount of memory could easily fit on just one memory board even with the high-speed, low density memory devices. Thus, we found that we could replace a small percentage of the memory with high-speed, low-density, high-cost memory and achieve most of the benefits that would result from the less practical solution of replacing all the memory. The processor can retain most of the lower speed and lower cost memory while taking advantage of the higher speed of the memory used where most of the activity takes place. This solution is possible because of the asynchronous nature of the processor to memory allowing variable access speeds. With this approach, the resulting PBX can accommodate over two times as many lines (of equivalent traffic per line) as prior to increasing the processing speed. This increase is achieved at a very small relative cost.

The fixed organization of programs and data between high speed and low speed main memory as proposed here is analogous to the organization between main memory and file memory described in [2]. One difference is that here we are allocating to main memory only. Comparison of our memory organization with classical main-memory organizations, e.g., parallel, cache, etc. will be presented, showing why our method was chosen for our PBX application.

The results of this effort are offered to the ITC because they address the problem of increasing real-time capacity with a method shown to be very simple and inexpensive but effective. The method is thought to be of general applicability.

REFERENCES

- [1] Z. Koono, A. Shoda, and Y. Tokita, "A Distributed Control System for Electronic Switching Systems," International Switching Symposium, 1976
- [2] K. Kusunoki and K. Yamamoto, "Optimum Program Design for Hierarchically Structured Memory in Electronic Switching System," Electronics and Communications in Japan, Vol. 59-A, No. 3, 1976