

MSMPS Packet Scheduling Algorithm for VOQ Switches

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Abstract—In this paper we present Maximal Size Matching with Permanent Selection (MSMPS) algorithm [1] which is responsibilities for circuit switching control. We discussed the general algorithm rules and circuit switching architecture which was used in our research. This switch architecture uses Virtual Output Queues (VOQ) for buffering incoming packets. MSMPS algorithm based on permanent connections between inputs and outputs. Simulations confirm that for large load our algorithm provides better efficiency than other algorithms.

I. INTRODUCTION

Requirements for today's communication networks are very high. Increasing number of users and more sophisticated applications require reliability and low delay during data transfer. At the same time QoS (Quality of Services) should be provided. In this fact the new generation nodes with high speed routers are designed. Very important things in this new infrastructures are buffering systems and algorithms which are used to control connections between inputs and outputs. In our research we based on switch architecture with Virtual Output Queues, which were first used and proposed in [2], [3].

In literature there are several good known scheduling algorithms. In this paper we compared Permanent [4], Random [4] and iSLIP [5] algorithms with presented MSMPS algorithm.

This paper is organized as follows. In second section switch architecture is presented. In the third section description of the MSMPS algorithm is given. The fourth section is dedicated for the simulation results. At the end of this paper conclusions are given.

II. SWITCH ARCHITECTURE

The general, studied switch architecture used in this paper is shown in Figure 1. Each input has separated buffer which is divided into N independent VOQs. In general case, the VOQs number is N^2 . Each virtual queue is denoted by VOQ (i, j), where i is the input port number and j is the output port number. It can be assumed that: $0 \leq i \leq N-1$ and $0 \leq j \leq N-1$.

III. SCHEDULING ALGORITHM

MSMPS algorithm based on permanent connections between inputs and outputs. Four connections pattern, in 4×4 switch, in each time slot are presented in Figure 2.

From Figure 2 can be observed that in each time slot, we have different connections pattern. Total combinations number is N , where N is a number of inputs and outputs. We assumed

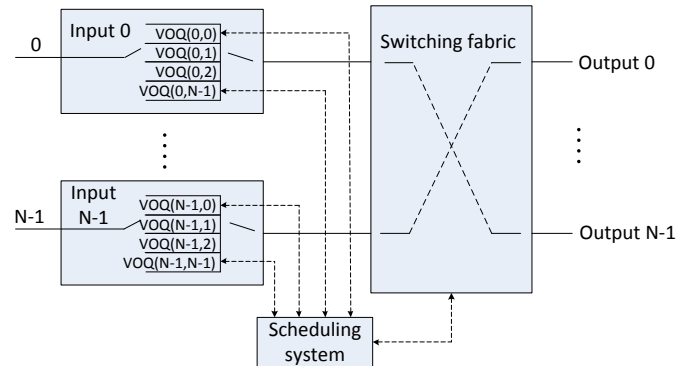


Fig. 1. Switch architecture

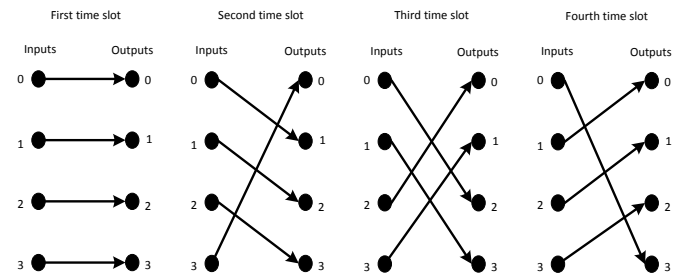


Fig. 2. Permanent connections pattern in each time slot

that presented switching fabric is symmetrical, which means that number of inputs and outputs are equal.

The most important element in our switch architecture is scheduling system which has information about number of packets, waiting in each buffers, to be send through the switch. Based on this information, Matrix of Queue Lengths (MQL) has been created. Figure 3 shows the way, how the MQL matrix is created and organized. More details about MQL matrix was presented in [1].

After matrix filled, MSMPS algorithm marks all positions in this matrix, according to permanent matching in the current time slot. All connections between inputs and outputs are classified into two groups. First one is empty connections group which contains all connections where there is no packets to be send. Second group is non-empty connections group, where belong connections with packets to be sent through the switch. Algorithm tries to find better connections pattern with the lowest number of empty connections. Algorithm was presented in details in [1].

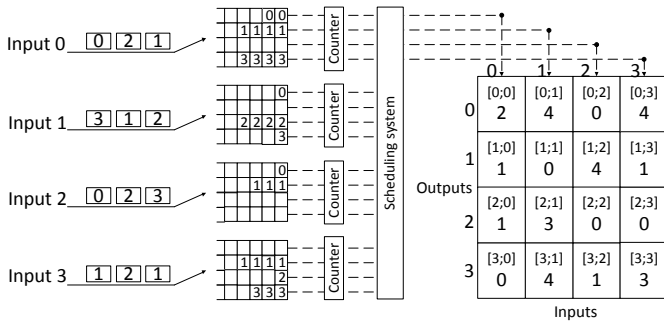


Fig. 3. Filling the MQL matrix

IV. SIMULATION RESULTS

The MSPMS algorithm was compared with other by using computer simulations. The results introduced in this paper are presented for 32×32 switches with VOQs of infinite size. The performance of presented algorithm was simulated under Bernoulli arrivals. Probability of the packet arrival is p , where $p \in (1 < p \leq 1)$ [6], [7]. Packet directed to suitable outputs were distributed uniformly. In simulation we assumed that one packet may occupied one time slot and only one packet may arrive at the input in the given time slot. It was assumed that switching network is non-blocking. In the simulations two parameters have been compared:

1) Efficiency was calculated as the difference between number of cells passed in n time slot through the switch to the number of cells which arrive to the switch in n time slot [1]. The efficiency in 32×32 switch for Bernoulli packet arrivals is shown in Figure 4. The MSMPS algorithm achieves 100% throughput for the load below 0.9. Above 0.9 traffic load, the efficiency decrease but achieves better results than the rest of compared algorithms.

2) Mean Time Delay (MTD) is measured as a quotient. Numerator is a difference between the time a packet arrive to the VOQ and the time when the same packet is transferred by the switch to its output port. Denominator is a packet length [1]. The MTD in 32×32 switch is plotted in Figure 5. It can be observed in Figure 5, when the traffic load is growing the MTD also grows. For the low traffic load, MSMPS algorithm

achieves lower MTD than the rest of algorithms, namely Permanent Random and iSLIP.

V. CONCLUSION AND FURTHER WORKS

In this paper we have presented the general MSMPS algorithm rules and switch architecture which was used to our research. Simulation results confirm that MSMPS algorithm achieves better efficiency than other known algorithms.

In future work we want to present our algorithm for unbalanced traffic and for bigger switch size. The most important thing is to improve efficiency for high traffic load. To achieve this objective we want establish non-empty connections pattern for more than one time slot. This solution will be presented in the next paper.

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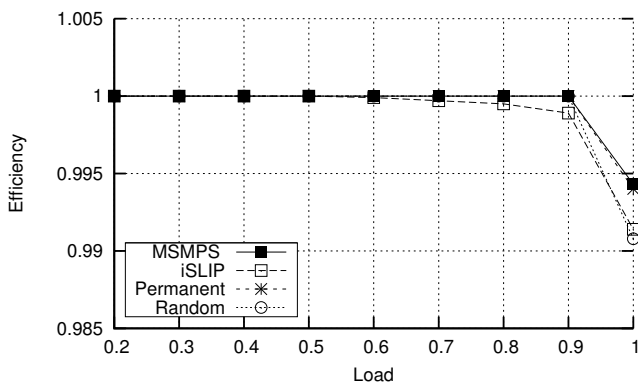


Fig. 4. The Efficiency in 32×32 switch for Bernoulli packet arrivals with destination uniformly distributed over all outputs

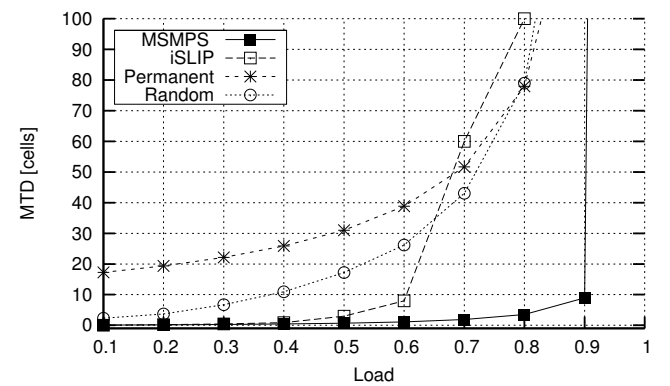


Fig. 5. MTD in 32×32 switch for Bernoulli packet arrivals with destination uniformly distributed over all outputs